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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,558	WATERMAN, JOHN KARL	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 7 - 9, 25, 26, 31, 32, 37 - 40, 46 – 52, 56 – 59, and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Albu et al., USPN 6,496,173 B1.

Claim 1, 37

Albu teaches a system using a current controlled charging circuit for charging columns of a liquid crystal display. Albu, col. 1, line 66 – col. 2, line 1. The system comprises a liquid crystal display (LCD) [reflective liquid crystal display (RLCD)] having a matrix of liquid crystal pixels comprising a plurality of columns and a plurality of rows with an intersection of a row and a column defining a location of a pixel. Albu, col. 1, lines 11 – 13. Albu teaches a digital-to-analog converter (DAC) [Integrating Digital-to-Analog Converter (IDAC) 34] adapted to receive digital inputs representative of pixel gray scales. The DAC has an output adapted for charging each of the plurality of columns to voltages representing the pixel gray scales. The output comprises current source pulses [waveform 42] that charge each of the plurality of columns to the voltages. Albu, col. 3, lines 1 – 24; col. 4, lines 3 – 21; and figures 2 and 3. As shown in figure 3, the current pulse has an amplitudes and a pulse-width.

Claim 7 - 9, 38 - 40

Albu teaches a gray scale current pulse look-up table [LUT located within a RAM module 32] adapted for converting the pixel gray scales into the digital inputs received by the DAC. Albu, col. 2, lines 5 – 8; col. 3, lines 12 – 14; and figure 2.

Claim 25, 26, 31, 32

Albu teaches that the control circuit 30, including the IDAC 34 and the look-up table 32, are fabricated on a semiconductor integrated circuit. Albu, col. 3, lines 60 – 64; and figure 2.

Claim 46 – 48, 56 – 59, 64

Albu teaches a comparator circuit for comparing the voltages representing the pixel gray scales with the voltages from the ADC. Albu, col. 49 – 54.

Claim 49

Albu teaches a method using a current controlled charging circuit for charging columns of a liquid crystal display. Albu, col. 1, line 66 – col. 2, line 1. The method comprises providing a liquid crystal display (LCD) [reflective liquid crystal display (RLCD)] having a matrix of liquid crystal pixels comprising a plurality of columns and a plurality of rows with an intersection of a row and a column defining a location of a pixel. Albu, col. 1, lines 11 – 13. Albu teaches charging with a current controlled charging circuit each of the plurality of columns to voltages representing pixel gray scales. Albu, col. 3, lines 1 – 24; col. 4, lines 3 – 21; and figures 2 and 3.

Claim 50

Albu teaches that the current controlled charging circuit is a current output digital-to-analog converter (DAC) [Integrating Digital-to-Analog Converter (IDAC) 34]. Albu, col. 3, lines 1 – 24; col. 4, lines 3 – 21; and figures 2 and 3.

Claim 51

Albu shows that the matrix of pixels is selectively coupling to the plurality of columns. Albu, figure 2.

Claim 52

Albu teaches that the step of charging is done with current pulses. Albu, col. 3, lines 1 – 24; col. 4, lines 3 – 21; and figures 2 and 3

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 - 4, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Kida et al., USPN 6,459,395 B1.

Claim 2

Albu does not specifically teach that a plurality of row switches selectively couples the matrix of pixels to the plurality of columns.

Kida teaches that a plurality of row switches [TFT 21 as a switching element] selectively couples the matrix of pixels 20 to the plurality of columns [column lines $25n$-1, $25n$, $25n$+1.] Kid, col. 3, lines 54 – 63; and figure 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the row switch configuration as taught by Kida with the system taught by Albu. Kida invites such combination by teaching,

> In recent years, liquid crystal display units tend to have a digital interface drive circuit integrally formed on the same panel as a pixel assembly. In the liquid crystal display units with the integral drive circuit, the pixel assembly comprises a matrix of pixels using polysilicon TFTs (thin-film transistors) as switching elements, and a horizontal drive system and a vertical drive system are disposed around the pixel assembly. The horizontal and vertical drive systems comprise TFTs and integrally formed with the pixel assembly on the same substrate (hereinafter referred to as "LCD panel").
>
> One serious problem with the fabrication of the above liquid crystal display units with the integral drive circuit is that the digital interface drive circuit integrally formed on the LCD panel takes up a large area around the pixel assembly (such an area will hereinafter be referred to as "frame"). Particularly, in liquid crystal display units with an integral drive circuit which has a reference-voltage-selection-type D/A converter, the D/A converter takes up a large area which poses a significant problem on efforts to make the frame of LCD panels smaller.
>
> Specifically, the reference-voltage-selection-type D/A converter comprises transistor switches between reference voltage lines which supply a plurality of reference voltages and a column line of the pixel assembly and the switch portions take up a large area in the D/A converter. Since there are required as many reference voltage lines as the number of gradations, these reference voltage lines take up a large area, i.e., the reference voltage lines extending up to the D/A converter in the LCD panel take up a large area. This large area presents an obstacle to attempts to reduce the size of the frame of LCD panels, and is responsible for making it difficult to increase the number of gradations.

Kida, col. 1, lines 13 – 45. Kida then adds,

> It is therefore an object of the present invention to provide a D/A converter which allows the frame of a display panel to be reduced in size, and a display unit which includes such a D/A converter.

Kida, col. 1, lines 49 – 50.

Claim 3

Albu teaches that a plurality of column switches [OTAs 36] selectively couples the output of the DAC to each of the plurality of columns. Albu, col. 3, lines 1 – 24; and figure 2.

Claim 4

Kida teaches that a column control logic [first and second horizontal drive systems 12 and 13] controls the plurality of column switches and row control logic [vertical drive system 14] controls the plurality of row switches. Kida, col. 3, lines 21 – 53; and figure 1.

Claim 27

Kida teaches that the plurality of column switches are fabricated on a semiconductor integrated circuit. Kida, col. 1, lines 13 – 23; and col. 3, lines 21 – 30. Albu teaches that the plurality of row switches are fabricated on a semiconductor integrated circuit. Albu, col. 3, lines 60 – 64; and figure 2.

Claim 28

Kida teaches that the column control logic and the row control logic are fabricated on a semiconductor integrated circuit. Kida, col. 1, lines 13 – 23; and col. 3, lines 21 – 30.

5. Claims 5, 6, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Kida et al. as applied to claim 2 above, and further in view of Glen et al., USPN 6,067,083.

Claim 5

Neither Albu nor Kida teach an LCD-pixel matrix address controller adapted for controlling the column and row control logic.

Glen teaches LCD-pixel matrix address controller [address generation unit 14] adapted for controlling the column and row control logic. Glen, col. 2, lines 34 – 51; and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the matrix address controller as taught by Glen with the system of Albu and Kida. Glen invites such combination by teaching,

> This invention relates generally to video graphics circuits and more particularly to selective enabling of a palette DAC in video graphics circuits to reduce power consumption of a video graphics circuit.

Glen, col. 7 – 10. Glen adds,

> It is a never-ending design challenge to reduce power consumption for all types of products. The design challenge is even greater for portable devices such as laptop computers, pagers, cellular telephones, etc. In such devices, power saving techniques are balanced with advanced feature sets that consume power. Typically, the more advance the feature sets that a portable device supports, the more power it consumes. Thus, design engineers of portable devices are constantly working to reduce the power consumption of advanced feature sets with minimal affects on the performance of the feature set.
>
> In general, video graphics circuits, which are utilized in portable computers, personal computers, television sets, and computer game devices, continually process pixel information from video data. This is true regardless of whether the raster is in the active display area (i.e., there is video data to be processed) or when the raster is in an inactive overhead area, which is required for synchronization signals and retrace times. As is known, the video data consists of a plurality of lines, which make up a frame (or field for interlaced display) of video, and may be for two-dimensional graphics, three-dimensional graphics, still images captured by a camera, and/or moving images captured by a camera. One frame/field of video data provides a display screen worth of information for one cycle of the image rate of the display. For example, if the image rate is sixty (60) frames/fields per second, the frame/field is presented for one-sixtieth of a second. The plurality of lines includes the video information (i.e., the information that will

> be presented on the screen), horizontal retrace, and vertical retrace (i.e., the overhead information). The horizontal retrace is used to provide horizontal synchronization of the video display and the vertical retrace is used to provide vertical synchronization of the video display.
>
> In typical video processing circuits, when the horizontal retrace and vertical retrace are occurring, the pixel generation circuit of the video graphics circuit is still active with a running clock even though no video data will be displayed. Since the horizontal retrace and the vertical retrace account for significant portion of the frame/field time (e.g., up to 25% or more), the pixel generation circuit is overworked by a corresponding percentage. As such, the power consumed by the pixel generation circuit during the horizontal and vertical retraces is wasted energy, resulting in a non-optimum video graphics circuit.
>
> Therefore, a need exists for a method and apparatus that reduces power consumption in video graphics circuitry by selectively disabling the pixel generation circuit.

Glen, col. 1, lines 14 – 62.

Claim 6

Glen teaches a video frame to LCD pixel matrix address logic [display controller 12] coupled to the LCD pixel matrix address controller, the video frame to LCD pixel matrix address logic adapted to receive video information and generate LCD pixel matrix addresses for the LCD pixel matrix address controller. Glen, col. 2, lines 34 – 51; and figure 1.

Claim 29, 30

Glen teaches that the LCD pixel matrix address controller [address generation unit 14] and the video frame to LCD pixel matrix address logic [display controller 12] is fabricated on a semiconductor integrated circuit. Glen, col. 2, lines 34 – 51.

6. Claims 10 – 12, 33, 34, 41 – 43, 54, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Briggs, USPN 5,103,112.

Claim 10, 41, 54

Albu does not specifically teach a pulse-width time control circuit or a step for controlling the pulse-widths of the current source pulses.

Briggs teaches a pulse-width time control circuit for controlling the pulse-widths of the current source pulses. Briggs, col. 1, lines 6 – 13; and col. 2, lines 28 – 37.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pulse-width time control circuit of Briggs with the system as taught by Albu. Briggs invites such combination by teaching,

> The field of this invention relates generally to variable width pulse generators. It has particular application for providing control pulses with relatively fast transitions using relatively slow devices, as for example amorphous silicon thin-film transistors. One application of the invention is in the driver circuitry of liquid crystal displays having its drive electronics integrated on the display matrix substrate.

Briggs, col. 1, lines 6 – 13. Briggs adds,

> Frequently it is desired to generate variable width pulses with a minimal amount of circuitry. For example, in certain liquid crystal display (LCD) devices, digital-to-analog converter circuits are formed using variable width pulse generators. Display information represented by binary numbers are converted into variable width pulses which pulses are used to control the conduction times of switching transistors. A ramp voltage is applied to one electrode of the switching transistor, the other electrode being coupled to a display element. The transistor is conditioned to conduct at predetermined intervals and is turned off as a function of the variable width pulse. At the time the transistor is turned off, the ramp voltage, and thus the potential applied to the display element is proportional to the binary value controlling the pulse width. (See for example U.S. Pat. Nos. 4,742,346 and 4,766,430 Gillette et al. which are incorporated herein by reference.)
>
> Display devices of this type may include many hundreds of such digital-to-analog converters and thus many hundreds of variable width pulse generators, requiring that such circuit elements be parts efficient. In addition, the circuitry may be fabricated with material having low carrier mobility such as amorphous

> silicon. In this latter instance special circuit configurations are necessary to overcome speed limitations incurred by the low carrier mobility.

Briggs, col. 1, lines 16 – 42.

Claim 11, 42, 55

Albu teaches that the time control circuit or step is coupled to a gray scale current pulse look-up table. Albu, col. 3, lines 11 – 24; and figure 2.

Claim 12, 43

Albu teaches that the control circuit is synchronized with a column clock. Albu, col. 3, lines 11 – 12. Briggs teaches that the pulse-width time control circuit is synchronized with a clock pulse generator 91. Briggs, col. 2, lines 11 – 24.

Claim 33 and 34

Albu teaches that the gray scale current pulse look-up table is fabricated on a semiconductor integrated circuit. Albu, col. 3, lines 60 – 64. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the pulse-width time control circuit on the semiconductor integrated circuit to ease manufacture and decrease space.

7. Claims 13, 14, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Briggs as applied to claim 10 - 12 above, and further in view of Izumikawa, USPN 5,970,106.

Claim 13, 44

Neither Albu nor Briggs teach a phase-locked-loop (PLL).

Izumikawa teaches a PLL that is adapted to synchronize clock input into a pulse-width time control circuit. Izumikawa, col. 1, lines 7 – 13; col. 2, line 58 – col. 3, line 7; and figure 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the PLL as taught by Izumikawa with the system as taught by Albu and Briggs. Izumikawa invites such combination by teaching,

> A PLL circuit is generally used in a microprocessor to generate a higher frequency clock signal from a lower frequency reference signal, the clock signal being in synchronism with the reference signal.

Izumikawa, col. 1, lines 15 – 18. Izumikawa adds,

> It is an object of the present invention to provide a digital PLL circuit wherein both the frequency acquisition and phase acquisition are obtained in a common signal mode without switching, and accordingly, wherein a switching circuit is not necessary.
>
> It is another object of the present invention to provide a phase/comparator block for use in the digital PLL circuit as described above.

Izumikawa, col. 1, lines 49 – 57.

Claim 14, 45

Izumikawa teaches that the PLL generates the clock input to the pulse-width time control circuit. Izumikawa, col. 2, line 58 – col. 3, line 7; and figure 2.

8. Claims 15 – 18 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Suzuki et al., USPN 5,453,991.

Claim 15

Albu does not teach an analog-to-digital converter (ADC) for converting the voltages on the columns to digital voltage values.

Suzuki teaches an analog-to-digital converter 144 for converting the voltages on the columns to digital voltage values. Suzuki, col. 12, line 59 – col. 13, line 9; and figure 16.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the ADC as taught by Suzuki with the system as taught by Albu. Suzuki invites such combination by teaching,

> The present invention relates to highly integrated electronic circuit devices and, more particularly, to an inspection circuitry for facilitating the operation tests for multiple-terminal semiconductor integrated circuit (IC) devices, each having an increased number of input/output terminal pins aligned at a decreased pitch. The present invention also relates to a technique of facilitating an operation test and/or a mounting state inspection for a semiconductor integrated circuit device for electrically driving a thin-plate type display device such as an active-matrix type liquid crystal display (LCD) unit.

Suzuki, col. 1, lines 7 – 17. After teaching the disadvantages of prior inspection system, Suzuki adds,

> The same goes with the inspection of operations of LCDs which have been applied extensively with the recent tendency toward smaller electronic devices. As the number of external connection terminal pads arrayed on a panel substrate increases, the conventional "probe inspection" scheme cannot achieve a satisfactory inspection. As terminal pads are arranged at higher density, it becomes more difficult to perform the pin-positioning alignment to bring all the probe pins into contact with the terminal pads at a time, thus resulting in the inspection reliability being decreased.

Suzuki, col. 1, line 62 – col. 2, line 4. Suzuki then teaches,

> It is therefore an object of the present invention to provide a new and improved inspection technique which can facilitate an operation test for a highly integrated multiple-terminal/small-pitch electronic device, while attaining an enhanced reliability.
>
> It is another object of the present invention to provide a new and improved highly integrated multiple-terminal/small-pitch electronic device which can facilitate an operation test therefor, while achieving an enhanced reliability.

Suzuki, col. 2, lines 8 – 16.

Claim 16

Suzuki teaches a digital comparator [image corrector 148] for comparing the voltages representing the pixel gray scales with the digital voltage values from the ADC. Suzuki, col. 12, line 59 – col. 13, line 9; and figure 16. See also Albu, col. 3, lines 25 – 32.

Claim 17

Suzuki teaches that comparisons of the voltages representing the pixel gray scales with the digital voltage values are used in determining compensation coefficients for each of the plurality of columns having different capacitance values. Suzuki, col. 12, line 59 – col. 13, line 9; and figure 16. See also Albu, col. 3, lines 45 – 59.

Claim 18

Suzuki teaches a memory 146 for storing the compensation coefficients. Suzuki, col. 12, line 59 – col. 13, line 9; and figure 16. See also Albu, col. 3, lines 45 – 59.

Claim 35

Suzuki teaches that the comparator and the ADC are fabricated on a semiconductor integrated circuit. Suzuki, col. 2, lines 17 – 28.

9. Claims 19 - 21, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Mori et al., USPN 5,668,650.

Claim 19

Albu does not specifically teach that each of the plurality of columns has substantially the same capacitance.

Mori teaches that each of the plurality of columns has substantially the same capacitance. Mori, col. 5, line 63 – col. 6, line 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the same capacitance as taught by Mori with the system of Albu. Mori invites such combination by teaching,

> When the gate-source capacitance Cgs of the TFT 3 differs row by row, the value of ΔV obtained from the equation (1) varies row by row. In the LCD device which uses the TFT panel shown in FIG. 9, the voltage holding characteristic of each pixel varies exposure area by exposure area, and varies row by row even in a single exposure area. When the same data signal is supplied to the individual pixels, the voltage held by each pixel varies exposure area by exposure area and row by row, causing display blurring.

Mori, col. 5, lines 52 – 61. Mori teaches the purpose of the invention.

> It is therefore a primary object of the present invention to provide a TFT panel whose thin film transistors all have the same gate-source capacitance, thereby contributing to providing an LCD device which has an excellent display quality without display blurring.
>
> It is another object of this invention to provide a TFT panel whose thin film transistors all have the same gate-source capacitance even when fabricated using partial exposure.

Mori, col. 5, line 63 - col. 6, line 4. Mori concludes,

> In short, according to the TFT panel embodying the present invention, even if the forming position of the source electrode SE varies due to an alignment error or misalignment during the manufacturing process, a change in main capacitance and a change in sub capacitance cancel out each other, so that the total gate-source capacitance does not change. The use of the TFT panel of this invention can provide an LCD device which allows the individual pixels to have the same voltage holding characteristic and has an excellent display quality without blurring.

Mori, col. 13, lines 1 – 10.

Claim 20, 60

Mori teaches that each of the plurality of columns is compensated to have substantially the same capacitance. Mori, col. 5, line 63 - col. 6, line 4.

Claim 21

Mori teaches at least one capacitor [capacitance compensation electrode CE] connected to some ones of the plurality of columns [source electrode SE] such that each of the plurality of columns has substantially the same capacitance as another column. Mori, col. 8, lines 26 – 35 and figure 1.

10. Claims 22, 23, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Mori et al. as applied to claim 19 - 21 above, and further in view of Shimada et al., USPN 6,081,250.

Claim 22

Neither Albu nor Mori teach at least one switch for coupling the at least one capacitor to the some ones of the plurality of columns.

Shimada teaches a column capacitance compensation circuit [capacitances 107a and 107 b] and at least one switch [analog switches 110a and 110b] for coupling the at least one capacitor to the some ones of the plurality of columns [source bus lines 102a and 102b]. Shimada, col. 4, lines 32 – 51 and figure 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the capacitance compensation circuit and switch as taught by Shimada with the system as taught by Albu and Mori. Shimada invites such combination by teaching,

> It is similarly an object of the present invention to reduce the effect of signal delay on display quality. In the invention, however, this object is achieved by completely different means for substantially extending the writing time.

Shimada, col. 2, line 66 – col. 3, line 2. Shimada concludes,

> In the embodiment, by installing two source bus lines for one pixel column, the pulse width of each gate bus line is set twice as long as one horizontal scanning period for driving in the state free from mixture of video signals but the effect of the embodiment is not limited to this case alone, and when more source bus lines are provided, the output pulse width of the gate bus line may be set as many times as the number of source bus lines per pixel column in one horizontal scanning period.
>
> Further in the embodiment, the writing time of video signal may be extended. By once converting the incoming video signal into a digital signal, storing the digital signal into a memory and converting the stored signal into an analog signal again at specific timing, the writing time of the video signal for each pixel may be extended. As a result, the required characteristic of the analog switch may be alleviated, and the writing characteristic of the video signal is further enhanced, so that the display quality may be more improved.

Shimada, col. 5, lines 49 – 67.

Claim 23

Shimada teaches a column capacitance compensation memory coupled to the column capacitance compensation circuit, the column capacitance compensation memory storing connection setting for the at least one switch for coupling the at least one capacitor to the some ones of the plurality of columns. Shimada, col. 5, line 58 – 67.

Claim 36

Albu teaches that the plurality of row switches are fabricated on a semiconductor integrated circuit. Albu, col. 3, lines 60 – 64; and figure 2.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Mori et al. as applied to claim 19 - 21 above, and further in view of Andrea et al., USPN 3,538,450.

Claim 24

Neither Albu nor Mori teach that a capacitor is a plurality of capacitors having capacitance values in a binary progression.

Andrea teaches a capacitor [binary capacitor 79] that is a plurality of capacitors having capacitance values in a binary progression. Andrea, col. 1, lines 14 – 24; col. 5, lines 1 – 20; and figures 1, 4 and 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the binary capacitor as taught by Andrea with the system as taught by Albu and Mori. Andrea invites such combination by teaching the advantages of a binary capacitor to provide a range of capacitance values.

> It has been found that in many applications, up to 20 db's of improvement is possible if fixed capacitors are employed to tune the master oscillator rather than tuned variable capacitors. The use of fixed capacitors for such a purpose, however, has presented many difficulties. Such difficulties include, among others, the problem of adding or subtracting capacitance from the master oscillator in small enough increments, and control means for causing such small increments of fixed capacitance to be either added or subtracted from the master oscillator in accordance with the particular need at a given time, and thirdly, the problem of obtaining phase lock. Phase lock presents a problem in that the addition or subtraction of discrete increments of capacitance in all likelihood will not result in the exact capacitance required to obtain and maintain phase lock.
>
> It is an object of the present invention to provide a stabilized master oscillator employing fixed capacitors rather than a tuned variable capacitance.

Andrea, col. 1, lines 45 – 63.

12. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al.

Claim 53

Albu does not specifically teach the step of controlling amplitudes of the current pulses.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the step of controlling amplitudes of the current pulses in view of Albu invitation to do so. Albu teaches,

> While waveform 42 is a constant amplitude current pulse, the actual waveform of the charging current applied can be any one of a variety of waveforms and is exclusively controlled by the LUT within RAM module 32.

Albu, col. 4, lines 16 – 19.

13. Claims 61 - 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Lien et al., USPN 5,940,057.

Claim 61 - 63

Albu does not specifically teach a circuit for setting the plurality of columns to a desired voltage before charging the plurality of columns to the voltages.

Lien teaches a circuit for setting the plurality of columns to a desired voltage before charging the plurality of columns to the voltages. Lien, col. 3, lines 25 – 47; col. 4, lines 25 – 34.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the charging circuit as taught by Lien with the system as taught by Albu. Lien invites such combination by teaching,

> The present invention is generally directed to a method and apparatus for eliminating cross-talk in liquid crystal display devices. More particularly, the

> present invention is related to a display device in which means for preventing cross-talk between data lines and pixels is provided.

Lien, col. 1, lines 10 – 14. Lien adds,

> It is a principle object of the invention to provide a liquid crystal display and a method of operating the display wherein crosstalk is reduced or eliminated.
>
> It is a further object of the invention to provide a circuit for driving the pixels of a liquid crystal display which utilizes the method.
>
> It is another object of the invention to reduce crosstalk in a liquid crystal display without increasing the cost or power required to drive the pixels.

Lien, col. 3, lines 15 – 24.

14. Claims 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albu et al. in view of Mori et al. as applied to claim 19 and 20 or as applied to claim 60 above, and further in view of Smit et al., USPN 6,151,238.

Claim 65, 66

Neither Albu nor Mori teach a fuse link connected plurality of capacitors.

Smit teaches a fuse link connected plurality of capacitors. Smit, col. 3, lines 15 – 20.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the fuse links connected to a plurality of capacitors as taught by Smit with the system as taught by Albu and Mori. Smit invites such combination by teaching,

> Therefore, what is needed is a more cost effective, simple and reliable system, method and apparatus for storing calibration information for the adjustment of internal functions without the limitations imposed by laser trimming, or requiring complex and expensive PROM.

Smit, col. 2, lines 27 – 32. Smit adds,

> The invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing in a single integrated circuit a programmable fuse array for storing calibration information used to adjust internal functions of the integrated circuit. This calibration information may be used to calibrate the internal functions of the integrated circuit to desired values for best operation thereof. In addition, the invention allows calibration of the internal functions and/or references after manufacture and assembly of a system utilizing the integrated circuit. The most efficient and cost effective use of mask programmed ROM firmware programs, for controlling a microcontroller in the integrated circuit, may be utilized with the present invention without affecting its post manufacture capabilities of storing the calibration information used to adjust the critical internal functions of the integrated circuit.

Smit, col. 2, lines 35 – 51. Smit further teaches,

> An advantage of the present invention is that external components are not required for post manufacture or field adjustment of critical parameters within the integrated circuit.
>
> Another advantage is lower cost implementation of integrated circuits requiring precision timing and/or voltage calibrated parameter values.
>
> Still another advantage is an integrated circuit utilizing lower cost mask programmable ROM, yet having the capability of precision adjustment of critical on chip circuit parameters.
>
> Yet another advantage is ease and low cost of manufacture of integrated circuits having adjustably precise features that may be calibrated at any time.
>
> A feature of the present invention is ease in post manufacture field adjustment of critical on chip parameter values without needing adjustable external components.

Smit, col. 3, lines 45 – 62.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Daubenspeck et al., USPN 6,496,053, teaches a fuse link using capacitance sensing for semiconductor devices.

Maurice, USPN 6,252,566 B1, teaches a compensation process for capacitance for a matrix display screen.

Dingwall, USPN 5,726,678, teaches a signal disturbance reduction arrangement for a LCD display.

Francis, USPN 5,841,411, teaches a cross talk compensation for a AMLCD display.

Hayashi, USPN 5,041,822, teaches row capacitors 18v that compensates for unwanted capacitance in an LCD display.

Uchino et al., USPN 5,959,600, teaches a voltage compensation device for an LCD.

Janssen et al., USPN 6,429,858 B1, and USPN 6,384,817 B1, teaches a DAC controlled ramp generator for an LCD device.

Albu et al., USPN 6,320,565 B1, teaches a DAC for an LCD device.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

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